

Исследование экосистемы процессоров Elbrus VLIW для вычислительного материаловедения: производительность и проблемы

Alexey Timofeev, Vladimir Stegailov



Contents

- Introduction of Elbrus processor
- Two libraries for fast Fourier transform
- Computational materials science code VASP
- Conclusions

Elbrus processor

Moscow Center
of SPARC Technologies

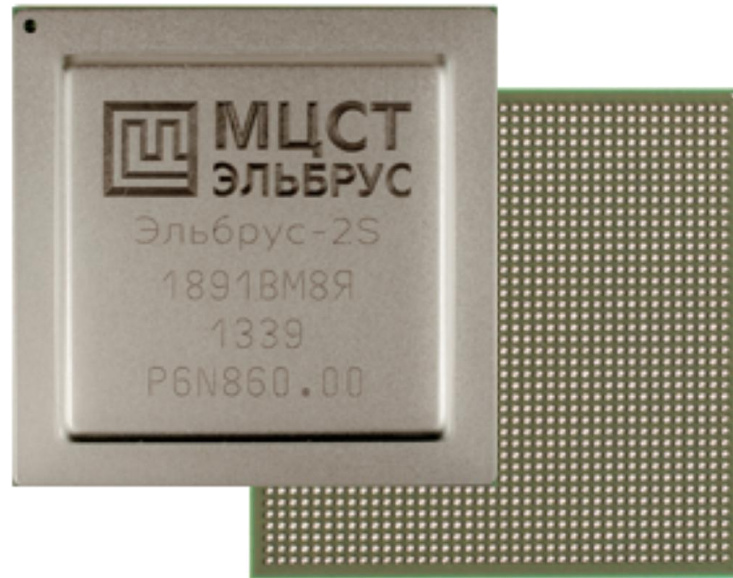


www.mcst.ru

Institute of Electronic Control Machines
named after I.S. Brook



www.ineum.ru



www.elbrus.ru

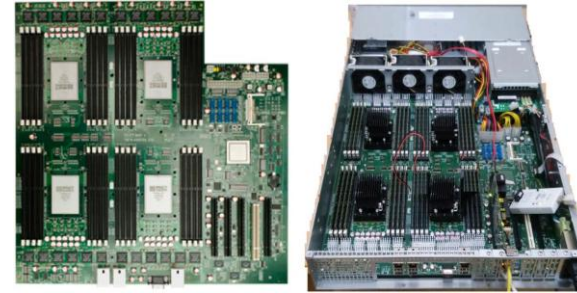
Elbrus processor

Moscow Center of
SPARC Technologies

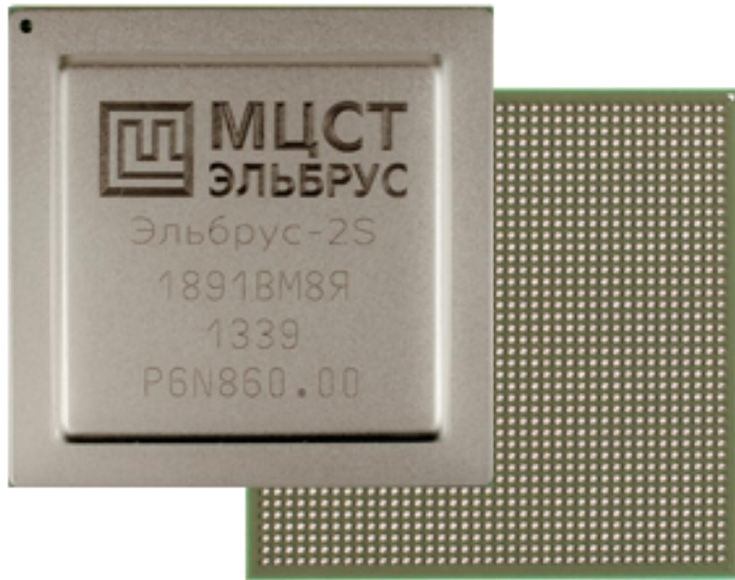
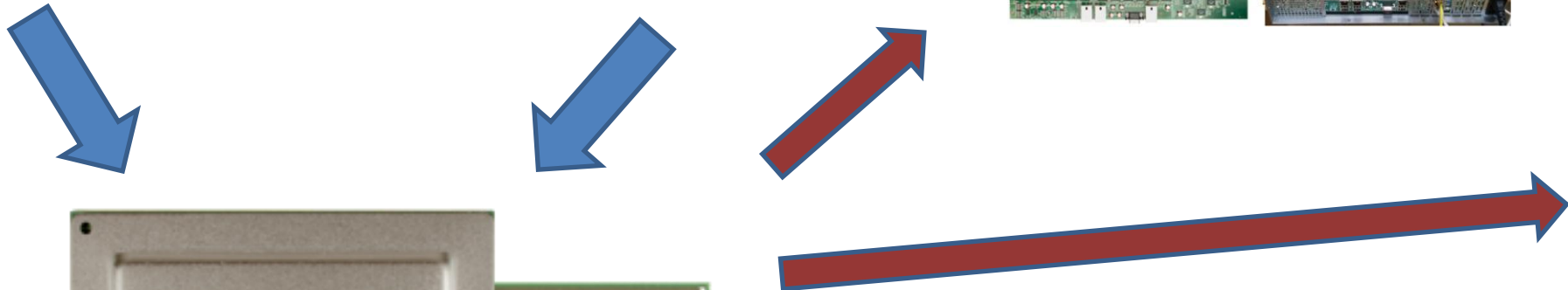


Institute of Electronic
Control Machines
named after I.S. Brook

Applications server



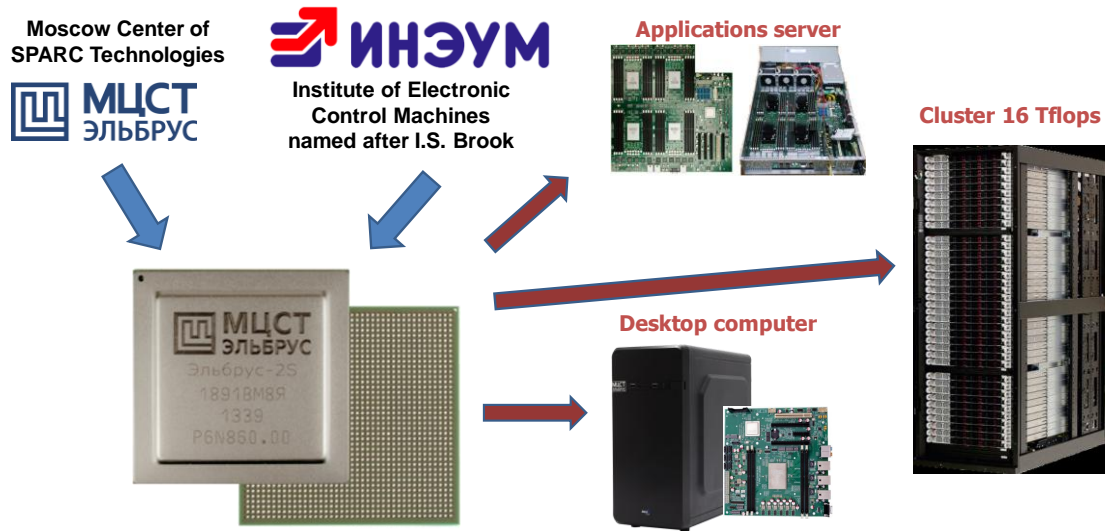
Cluster 16 Tflops



Desktop computer



Elbrus processor



Own development of

- BIOS
- Operating system
- Optimizing compilers from C, C ++, Fortran, Java, C #, Javascript and other instruments for programming
- Mathematical Libraries
- Tools for servers and clusters

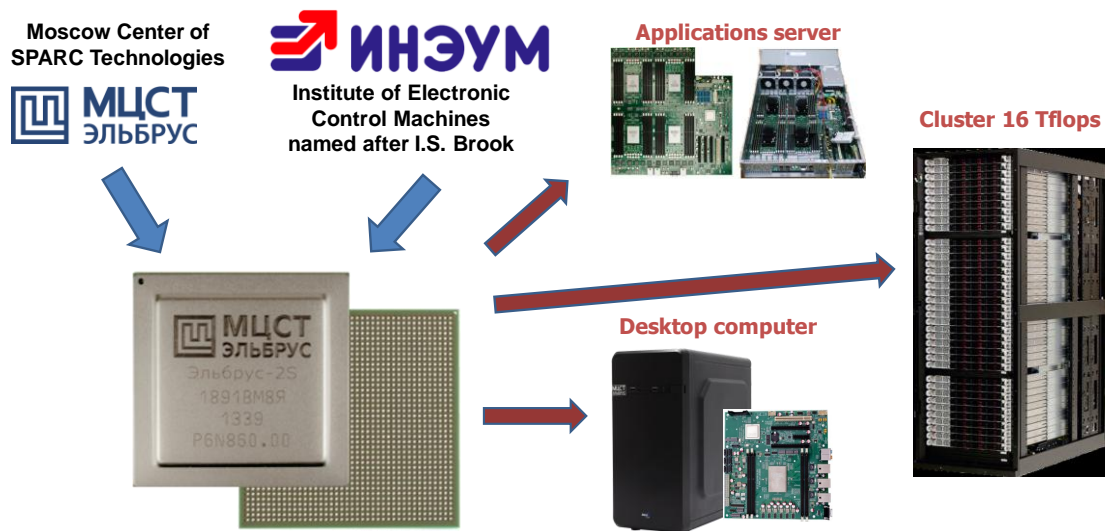
Parallel Energy Efficient Architecture

- 125 GFlops on 8 cores
- VLIW architecture
- High single-threaded performance
- General Purpose Processor

Effective binary compatibility with Intel x86, x86-64

- Execution of Windows XP, Windows 7 and above, Linux
- Compatibility layer for applications in x86 / x86-64 code in Linux

Elbrus processor



Own development of

- BIOS
- Operating system
- Optimizing compilers from C, C ++, Fortran, Java, C #, Javascript and other instruments for programming
- Mathematical Libraries
- Tools for servers and clusters

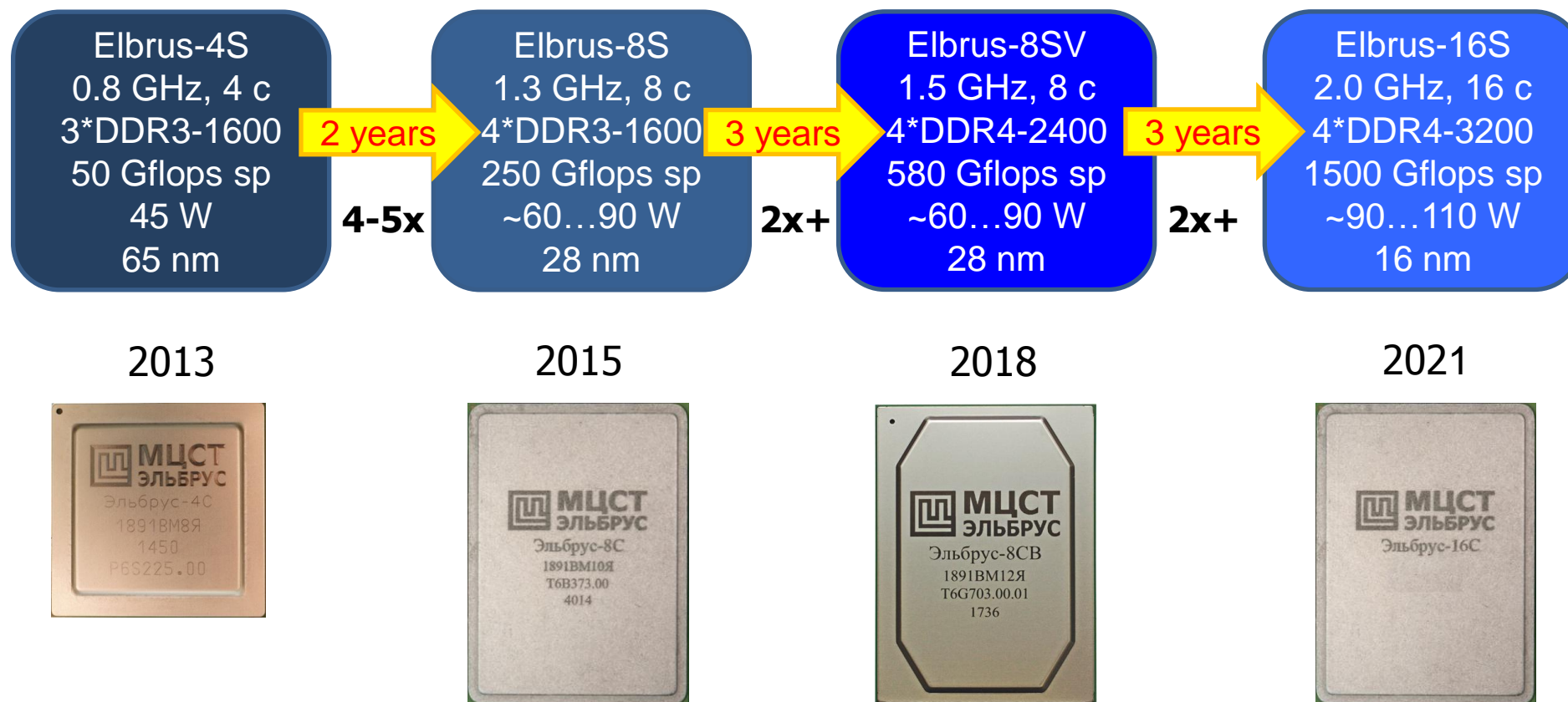
Parallel Energy Efficient Architecture

- **125 GFlops on 8 cores**
- **VLIW architecture (as Intel Itanium IA-64)**
- High single-threaded performance
- General Purpose Processor

Effective binary compatibility with Intel x86, x86-64

- Execution of Windows XP, Windows 7 and above, Linux
- Compatibility layer for applications in x86 / x86-64 code in Linux

Development of server multiprocessors "Elbrus"



On the basis of new multiprocessors computers and software are designed

Two libraries for fast Fourier transform

FFT Libraries

FFTW

- The most popular library
- It is considered the fastest
- Release 3.3.5 of July 31, 2016.

Contents and features:

- Multidimensional Fourier Transforms;
- $O(N \log N)$ for any sizes of the incoming array;
- Parallelism (Posix, OpenMP, MPI)

EML

(Elbrus Mult. Library)

- Own development of the MCTS

Content:

- vector arithmetic;
- linear algebra;
- signal processing;
- image and video processing;
- 2-D and 3-D graphics.

Two stages of the FFT algorithm



Initialization

FFTW via `fftw_plan_dft(..)`,
EML via `eml_Signal_FFTInit(...)`.

- once for a given array size



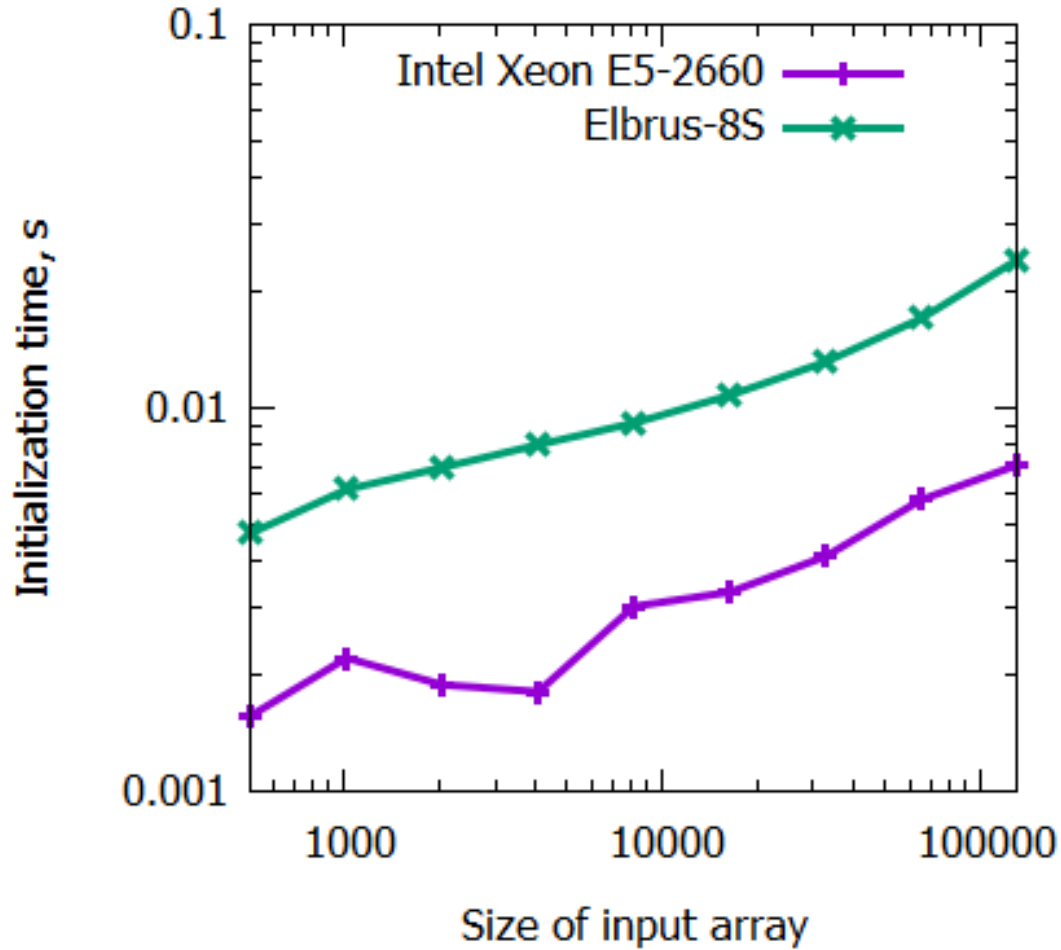
Execution

FFTW via `fftw_execute_dft(p,in,out)`,
EML via `eml_Signal_FFTFwd(...)`.

- one or many times

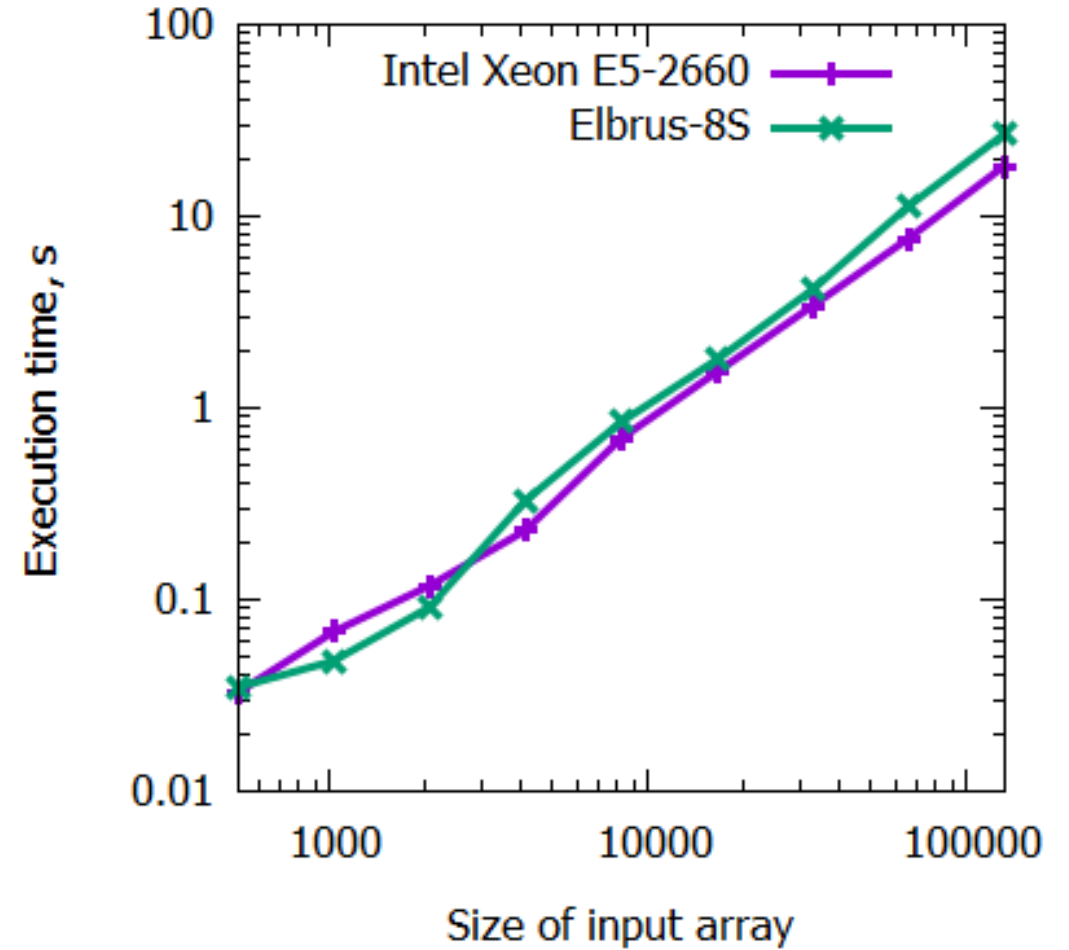
Intel Xeon E5-2660v4 (2.0 GHz) vs Elbrus-8S (1.3 GHz) for FFTW

Initialization



Intel is three times faster

Execution (1000 launches)

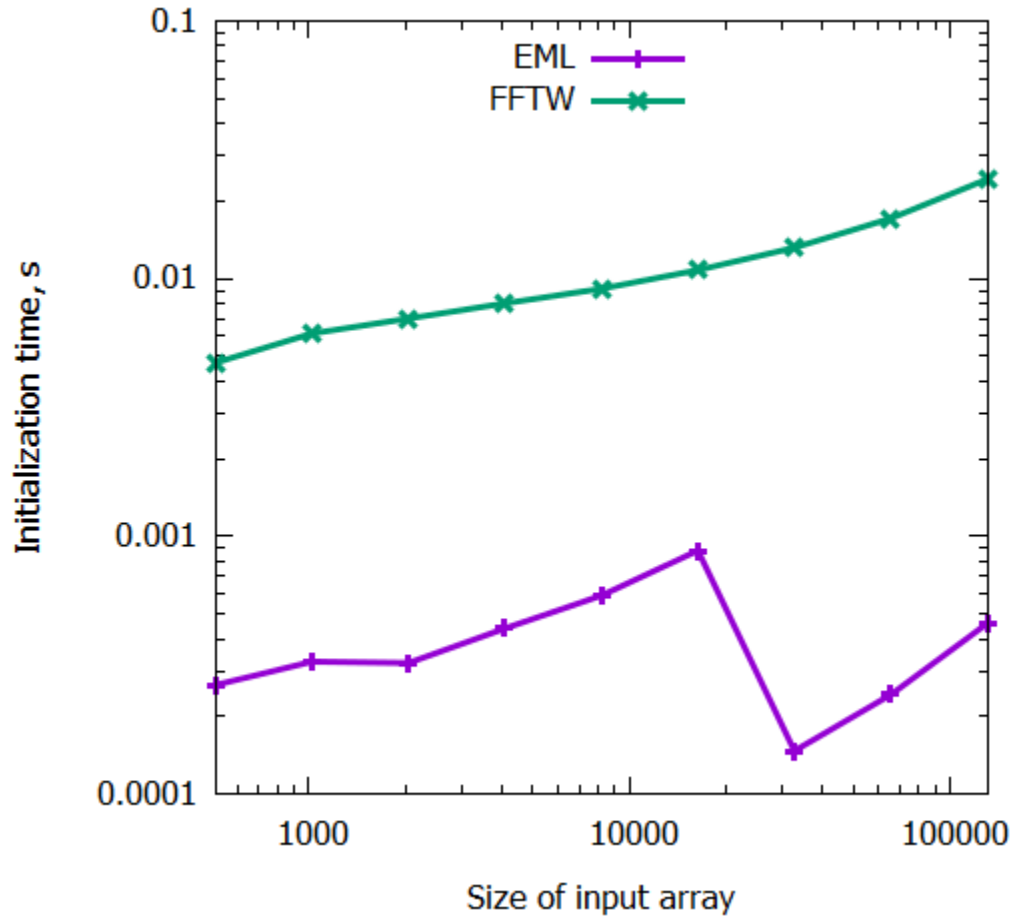


Processors are nearly equal

EML (Elbrus Math library) vs FFTW

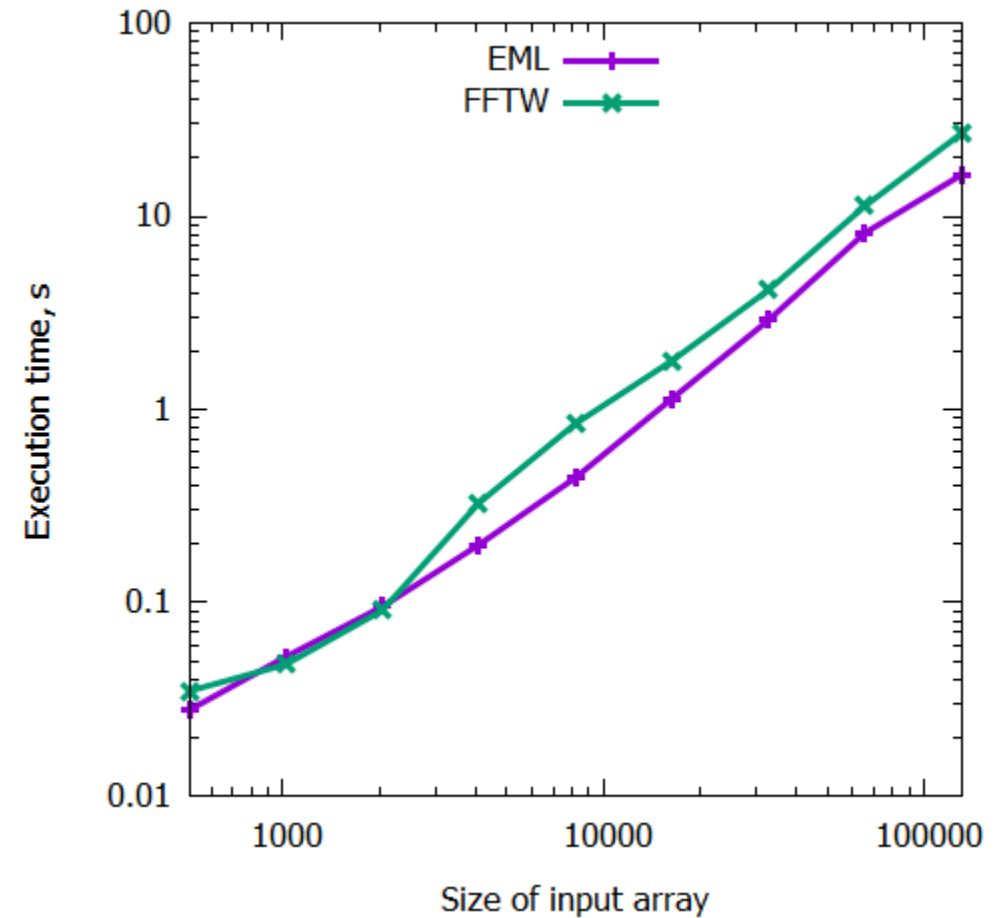
on Elbrus-8S

Initialization



EML initialization is ten times faster

Execution



EML is nearly equal to FFTW

**Computational materials science code VASP
on Elbrus-8S**

Computation materials science as supercomputer workload

- Example of statistics for the Edinburgh Parallel Computing Centre

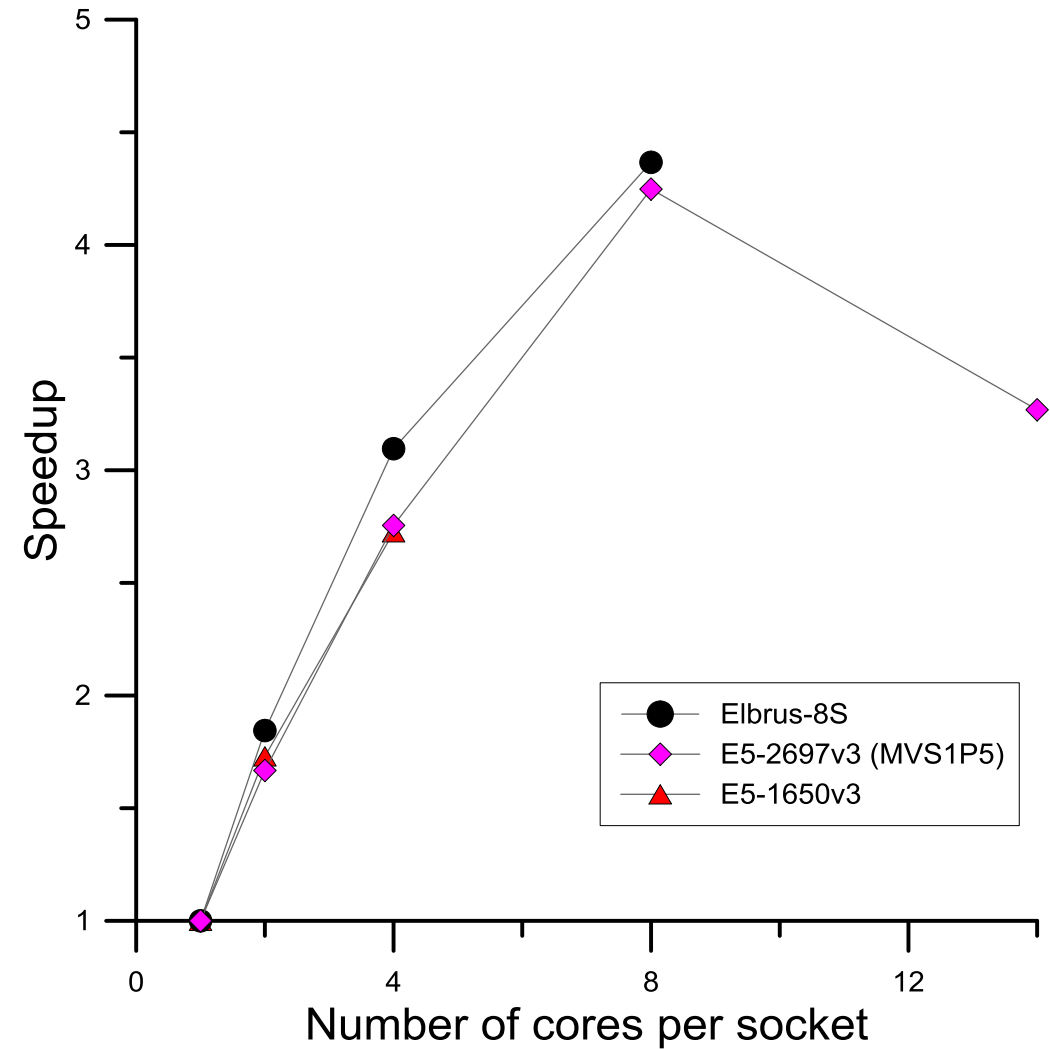
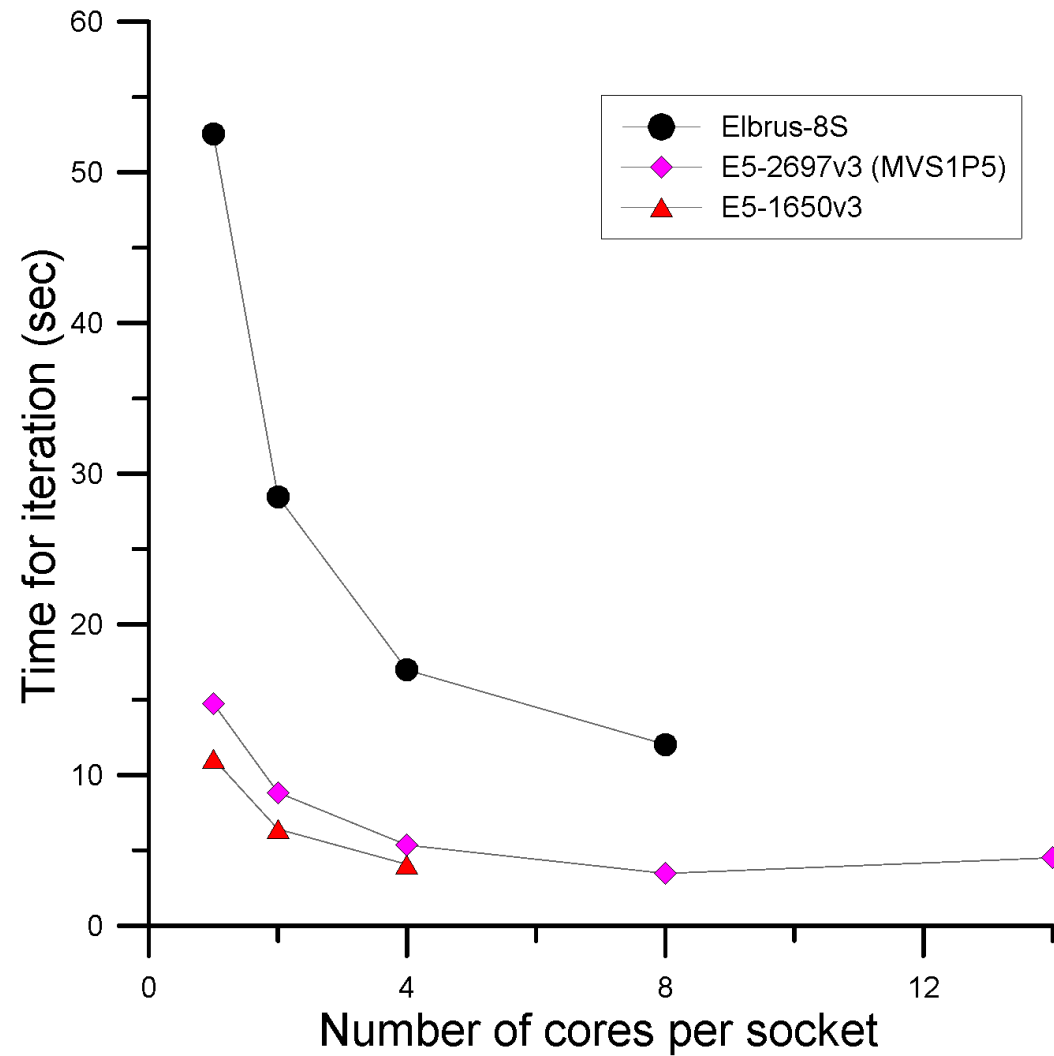
Code Usage on ARCHER (2014-15) by CPU Time:

Rank	Code	Node hours	Method
1	VASP	5,443,924	DFT
3	CP2K	2,121,237	DFT
4	CASTEP	1,564,080	DFT
9	LAMMPS	887,031	Classical
10	ONETEP	805,014	DFT
12	NAMD	516,851	Classical
20	DL_POLY	245,322	Classical

52% of all CPU time used by Chemistry / Materials Science / Biomolecular Simulation

The dependence of the time for the 1st iteration

of the liquid Si model test in VASP on the number of cores per socket



Our way to compare “apples” to “oranges” - i.e. different architectures

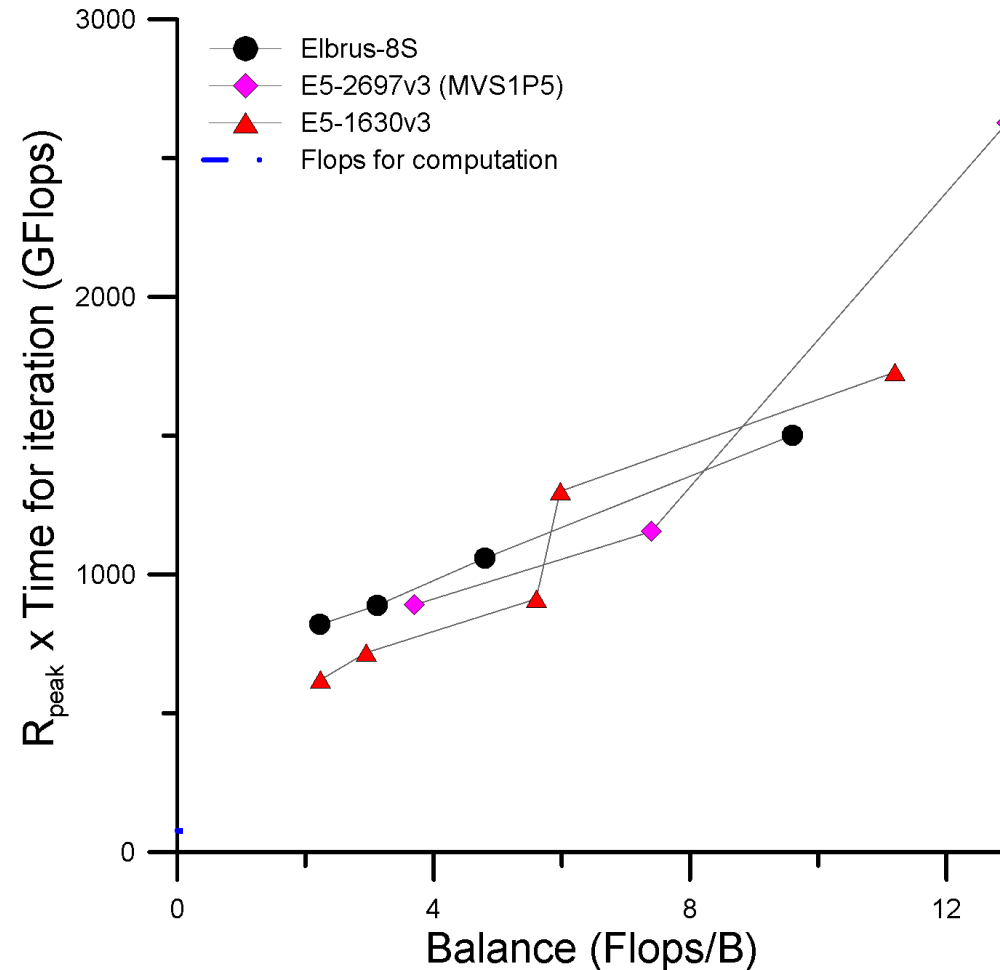
- We use reduced parameter to compare different architectures – number of FLOP that could be executed during computational time

$$\begin{array}{l} \text{Theoretical peak performance } (R_{peak}) \\ [\text{ FLOP / sec }] \end{array} \times \begin{array}{l} \text{iteration time VASP} \\ [\text{ sec }] \end{array} = \begin{array}{l} \text{Number of operations, that} \\ \text{could possibly be done} \\ \text{during iteration time} \\ [\text{ FLOP }] \end{array}$$

- We use balance parameter to characterize memory subsystem

$$\frac{\begin{array}{l} \text{Theoretical peak performance } (R_{peak}) \\ [\text{ FLOP / sec }] \end{array}}{\begin{array}{l} \text{Memory bandwidth} \\ [\text{ Megabytes / sec }] \end{array}} = \begin{array}{l} \text{Balance} \\ [\text{ FLOP / byte }] \end{array}$$

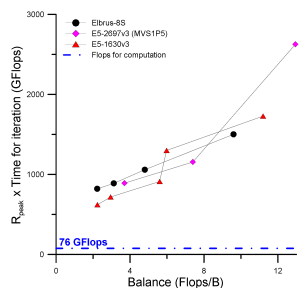
The dependence of the time for the first iteration of the liquid Si test on the number of cores per socket in the reduced parameters $R_{peak} \cdot \tau$ and balance B



Conclusions

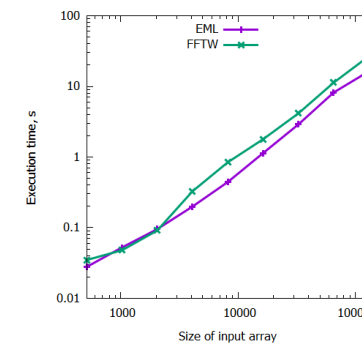
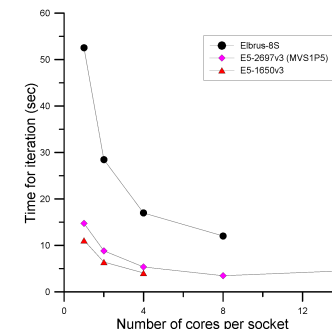
Hardware and software ecosystem of russian Elbrus processors are mature enough for material science calculations that has been checked on the example of VASP.

Elbrus-8S shows larger time-to-solution values, however there is no large gap between performance of Elbrus-8S and Xeon Haswell CPUs.



A new metric that allows us to compare the processors of different architectures is proposed

FFTW performance on Elbrus-8S is competitive with Intel Xeon Broadwell CPUs. EML on Elbrus-8S (1.3GHz) appears to be close or even more effective than FFTW on Intel Xeon E5-2660v4 (2.2 GHz).



References

1. Tyutlyayeva, E., Konyukhov, S., Odintsov, I., Moskovsky, A.: The Elbrus Platform Feasibility Assessment for High-Performance Computations, pp. 333{344. Springer International Publishing, Cham (2016). doi: 10.1007/978-3-319-55669-7_26
2. Kozhin, A.S., Polyakov, N.Y., Alfonso, D.M., Demenko, R.V., Klishin, P.A., Kozhin, E.S., Slesarev, M.V., Smirnova, E.V., Smirnov, D.A., Smolyanov, P.A., Kostenko, V.O., Gruzdov, F.A., Tikhorskiy, V.V., Sakhin, Y.K.: The 5th generation 28nm 8-Core VLIW Elbrus-8C processor architecture. Proceedings – 2016 International Conference on Engineering and Telecommunication, EnT 2016 pp. 86{90 (2017). doi: 10.1109/EnT.2016.25

The 5th Generation 28nm 8-Core VLIW Elbrus-8C Processor Architecture

Aleksey S. Kozhin^{1,2}, Nikita Yu. Polyakov^{1,2}, Daniil M. Alfonso¹, Roman V. Demenko^{1,2}, Pavel A. Klishin¹, Evgeniy S. Kozhin¹, Mikhail V. Slesarev¹, Elena V. Smirnova¹, Dmitriy A. Smirnov¹, Pavel A. Smolyanov¹, Vitaliy O. Kostenko¹, Feodor A. Gruzdov¹, Vladimir V. Tikhorskiy¹, Yuli Kh. Sakhin^{1,2}

¹AO "MCST"
Moscow, Russia

²Moscow Institute of Physics and Technology (MIPT)
Moscow, Russia

{Alexey.S.Kozhin, Nikita.Yu.Polyakov, Daniil.M.Alfonso, Roman.V.Demenko, Pavel.A.Klishin, Evgeniy.S.Kozhin, Mikhail.V.Slesarev, Elena.V.Smirnova, Dmitriy.A.Smirnov, Pavel.A.Smolyanov, Vitaliy.O.Kostenko, Feodor.A.Gruzdov, Vladimir.V.Tikhorskiy}@mcst.ru

Abstract—Elbrus is an explicitly parallel VLIW instruction set architecture developed by MCST. In this paper, we introduce the microarchitecture of the 5th generation 8-core Elbrus-8C processor implemented on 28nm. Elbrus-8C has 5x the peak performance for floating-point operations as compared with its predecessor, the Elbrus-4C processor, due to improved single-core performance and doubled number of cores. Microarchitecture enhancements include a 16 MB shared third-level cache, high-bandwidth, low-latency on-chip network, and a new cache coherence protocol. Elbrus-8C improves bandwidths of memory and I/O subsystems using four DDR3-1600 memory channels and a new 8 GBps full-duplex I/O link. The Elbrus-8C processor also offers energy saving, reliability, and die yield improvement mechanisms required due to large die area and power.

heterogeneous Elbrus-2C+ processor integrating two general purpose Elbrus-S cores and a third-party 4-core DSP cluster was produced [2]. In 2013 MCST released its fourth generation processor – quad-core Elbrus-4C processor.

The goal of the fifth generation Elbrus-8C processor was to achieve the performance of more than 150 single-precision GFLOPS and 75 double-precision GFLOPS, making it about 3 times faster than its predecessor Elbrus-4C. In order to meet the goal and achieve a balanced design the MCST team had to:

- improve floating-point performance of each processor core,
- integrate 8 cores on a single die, thus doubling the number of cores per die as compared with the previous design.

Характеристики процессоров Эльбрус-4С, 8С

	Эльбрус-4С	Эльбрус-8С
Тактовая частота	800 МГц	1300 МГц
Число ядер	4	8
Пиковая производительность микросхемы, Gflops (64 разряда, двойная точность)	25	125
Пиковая производительность микросхемы, Gflops (32 разряда, одинарная точность)	50	250
Кэш-память данных 1-го уровня, на ядро	64 КБ	
Кэш-память команд 1-го уровня, на ядро	128 КБ	8 * 512 КБ
Кэш-память 2-го уровня (универсальная)	8 МБ	16 МБ
Организация оперативной памяти	До 3 каналов DDR3-1600 ECC	DDR3-1600 ECC
Пропускная способность каналов оперативной памяти	38,4 ГБ/с	
Возможность объединения в многопроцессорную систему с когерентной общей памятью	До 4 процессоров	До 4 процессоров
Каналы межпроцессорного обмена	3, дуплексные	3, Каналы дуплексные
Пропускная способность каждого канала межпроцессорного обмена	12 ГБ/с	8 ГБ/сек
Площадь кристалла	380 мм ²	321 mm

Сравнение МП Эльбрус-16С с Intel Xeon

Микропроцессоры	Intel Xeon E7-4850 v4	Intel Xeon Platinum 8153	Эльбрус-16С
Микроархитектура	Broadwell	Skylake	Эльбрус v6
Тактовая частота (turbo), ГГц	2,8	2,0 (2,8)	2,0
Пиковая пр-ность, s/d (turbo), Гфлопс	1075/538	1200/600 (1600/800)	1500/750
Число ядер	16	16	16
Объем кэша, Мбайт	40	38	>32
Каналов памяти	4	6	>4
Пропускная способность памяти, Гбайт/с	85	119	>100
Многопроцессорность	До 4	До 8	До 4
Технолог. процесс, нм	14	14	16
Тепловой пакет, Вт	115	125	120
Год выпуска	2017	2017	2021

Сопоставим по основным характеристикам с самыми современными процессорами Intel Xeon, имеет преимущество за счет архитектуры ядра